Investigation of low noise, low cost readout electronics for high sensitivity PET systems based on Avalanche Photodiode arrays

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***Abstract*—**A compact, low noise and low cost readout system based on commercially available application-specific integrated circuits (ASICs) is under investigation. These front-end circuits have been used to readout a prototype detector module comprising Lutetium Oxyorthosilicate (LSO) scintillation crystals coupled to avalanche photodiode (APD) arrays. A major goal for this work is to build a dedicated high performance breast imaging PET system. Characteristics of signal response, noise, pedestals and gain of the chip have been evaluated. The channels have a linear response to within 2% across a ±75 fC dynamic range and have an intrinsic 120 e- rms noise level in each channel. The chips allow hardware adjustment of bias levels to allow gain uniformity of less than 5% for all channels within a chip. Initial tests of the chip when connected to a prototype APD array also showed good performance. 13% energy resolution was obtained with direct 5.9 keV x-ray interactions in a single APD pixel. The gain performance is very stable over all channels. Initial performance evaluation indicates that the chip has good performance and may be used as front-end electronics for the proposed PET system.

I. Introduction

There is a considerable demand in recent biomedical research to improve the spatial resolution of PET scanners [1-5]. The spatial resolution of PET imaging depends on limiting factors such as detector size, annihilation photon non-collinearity, and positron range [6]. Recent work [7,8] suggests that sub-millimeter spatial resolution can be achieved using compact and highly pixellated avalanche photodiode (APD) arrays coupled to fine LSO scintillation crystals. In order to maintain high detector signal-to-noise ratio (S/N), a novel detector configuration was proposed [8] that provides nearly complete (~95%) light collection efficiency for fine crystals. Based on this design, ultra-high resolution positron emission tomography (PET) systems are being developed for breast and small animal imaging.

This paper describes the investigation of readout electronics for the proposed PET detector arrays. The compact APD detector module comprises a relatively large number of channels that requires a low noise and low power integrated readout system. This work focuses in evaluating compact, low noise and low cost readout electronics based on commercially available multi-channel front-end Application Specific Integrated Circuits (ASICs) [9].

Manuscript received November 22, 2002. This work was supported in part by the Susan G. Komen Foundation under Grant No. IMG-0346 and the Whitaker Foundation under Grant No. RG-01-0492.

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II. Proposed PET System and Readout Requirements

Figure 1 depicts the proposed small PET systems, which are being developed for breast and small animal imaging. The PET system will be built using many 1-D detector modules, each consisting of a very thin (≤300μm) APD array coupled to a rectangular (1 mm thick) LSO crystal. These detector layers are stacked together and placed "edge on" with respect to incoming photons.

The prototype detector module uses an APD array that comprises of 41 rectangular elements, each with dimension of 0.7x7 mm^2 on a 1 mm pitch. The final APD array module will be ≤300μm thick, with more channels and higher compactness.

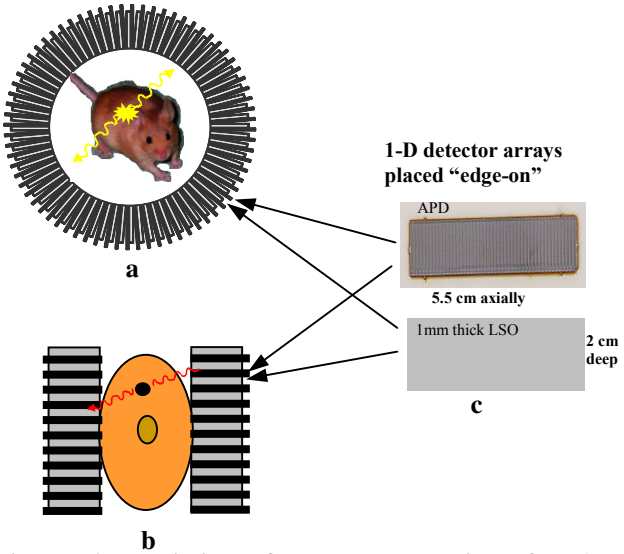

Figure. 1: Depiction of small PET designs for a) small animal and b) breast imaging systems c) prototype 1-D array detector module

In this prototype design, individual APD channel readout is selected in order to provide optimal spatial and energy resolutions. To efficiently manage a large number of channels

involved in the design and significantly reduce heat generation in the system, integration of many of the APD channels into a low power and low noise ASIC front-end chip optimized for the system is necessary. In this work, the possibility of utilizing commercially available multi-channel front-end chips is investigated in order to significantly reduce the development time and cost.

III. Prototype Readout System Setup

A prototype multi-channel readout system has been setup as indicated in Figure 2. A prototype APD detector array is connected to a multi-channel readout board (IDEAS ASA), hosting two ASIC chips. Each ASIC chip consists of 32 input readout channels that can operate independently. The output from each channel is multiplexed and readout serially by a digitizer and control unit, which is monitored by a PC.

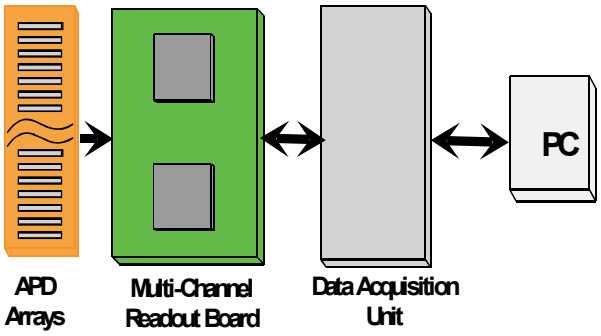

Figure 2: Prototype readout system setup

All channels can also be tested through a multiplexed input that allows injecting a test charge into a specific channel. External bias adjustment is provided for calibration purposes. In general, the system allows control and measurement of fundamental parameters of the chip, which includes pedestal, noise, and gain.

Supply Voltage	± 2V
Feedback resistor	Adjustable (~ 10M to 10G)
Input Device	PMOS referenced to gnd
Peaking time	2µS
Capacitive load	< 10 pF
Noise	100e + 15e/pF
Typical gain	~8.3 µA/ fC
Gain Range	< 10% of Mean
Pedestal Range	< 4.5% of full range

Table 1: VA/TA summary of specifications

IV. The Front-end ASIC chip

The front-end readout ASIC chip is based on the VA_TA chip series from IDE AS, Norway. A single VA_TA chip includes 32 channels of a parallel analog readout circuit followed by a corresponding analog trigger circuit. A summary of typical specifications for the selected chip is shown in table 1.

A single channel includes a low power charge-sensitive preamplifier/shaper, sample/hold and fast triggering circuits (Figure 3). The trigger chip includes a fast CR-RC shaper followed by externally adjustable level- sensitive discriminator. A signal above the threshold level generates a trigger signal, which is ORed to single trigger output. The trigger signal is sent to the analog chip to toggle the sample/hold circuits to sequentially sample and acquire data. The timing and signal acquisition sequence is depicted in Figure 4.

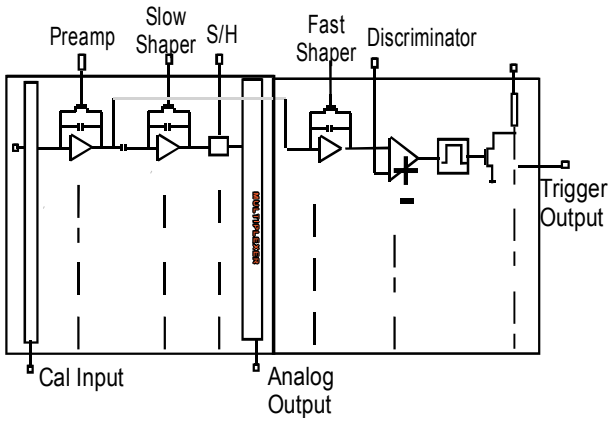

Figure 3: Front-end ASIC architecture

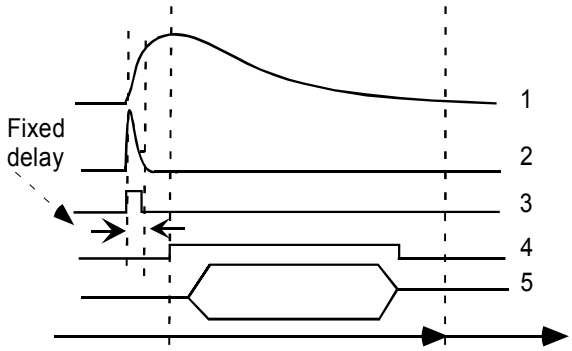

Figure 4: Signal acquisition sequence

V. ASIC Performance Measurements

Preliminary performance tests have been performed using an internal test pulse provided within the system. Figure 5 shows a semi-gaussian shaped signal response from a typical channel in the preamp/shaping circuit. The 2 μs peaking time is not optimal for LSO and will introduce unnecessary noise into the system. The noise performance of this circuit is comparable or better than most typical discrete charge sensitive preamplifier/shaper circuits currently available.

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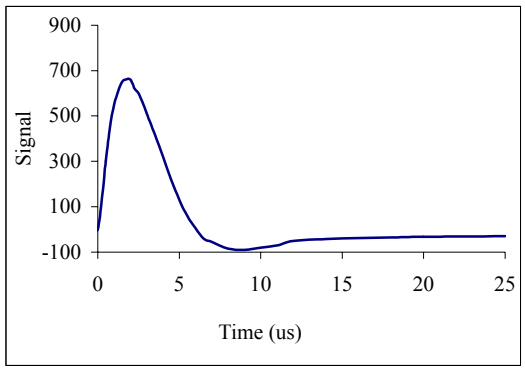

Figure 5: Preamp/Shaper signal response for one channel.

Figure 6 shows the noise and pedestal measurements for all channels. The values are obtained by a multiplexed readout sequence, where a hold is applied and a consecutive sampling of the shaped signals has been performed. The intrinsic noise of the chip is uniform over all channels to within ±10%. Pedestal spread is large but may be corrected in software. The pedestal represents the minimum detected pulse height for a given channel.

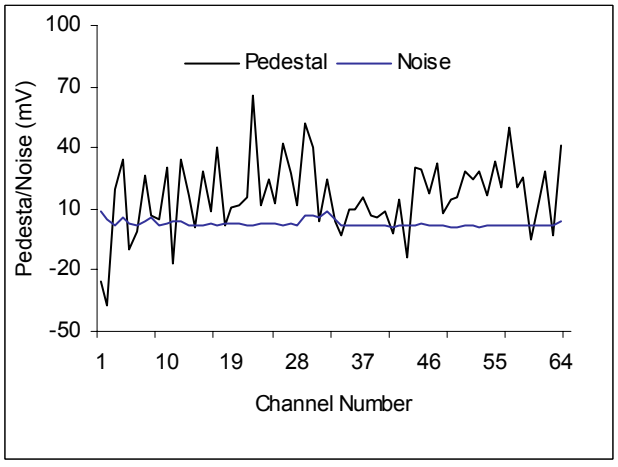

Figure 6: Pedestal and noise variation between ASIC channels without APD array connected.

External bias adjustment keeps the gain variation between channels in a single chip to less than 5%. There is a slight variation in gain between the two 32-channel circuits that may be corrected in post-processing.

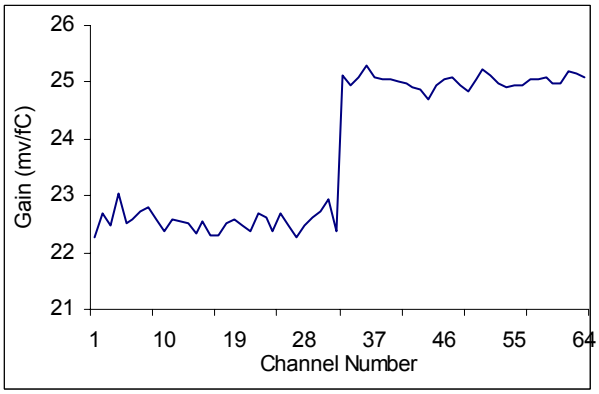

Figure 7: Gain variation between channels

The linearity for one channel of the system after calibration and selecting a suitable threshold was measured using an external test input charge to mimic an APD signal. The charge amplitude was obtained from the peak location in the pulse height spectrum. The response was linear to within 2% within a ± 50fC dynamic range (Figure 8).

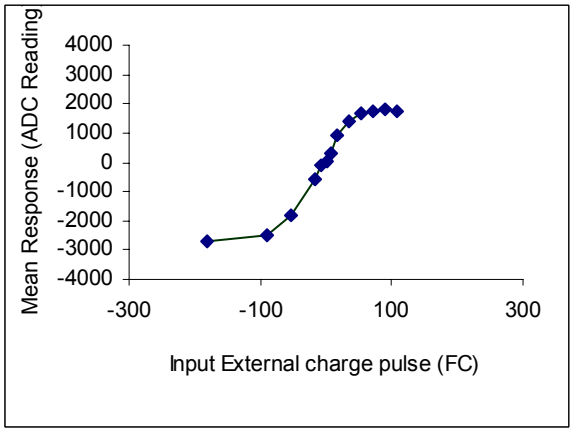

Figure 8: Linearity and dynamic range performance test

VI. Initial Tests and Results with APD Connected

Two different prototype 1-D APD arrays were used to perform basic performance measurement tests, using a 5.9 keV Fe-55 x-ray source. The first measurement was performed using a prototype APD array obtained from RMD, Inc. It consists of 41 APD elements, each with 0.7 x 7 mm^2 on a 1 mm pitch. At bias voltage around V_{bias}=1100V, it has a stable gain with dark current of about 50nA and capacitance of 0.7pf/mm^2 [8].

In this particular test, eight APD elements (channels) were used, each connected to the front-end ASIC using ac coupling due to the relatively high leakage current of the APD. The

response of all channels superimposed is shown in Figure 9. The plot shows that uniformity between channels is maintained with less than 5% gain variation, even when the APD array is connected to the ASIC.

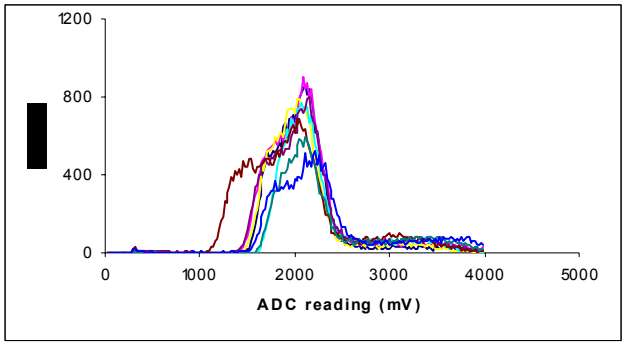

Figure 9: Measured x-ray spectra in 8 APD channels

A second prototype APD array was obtained from Advanced Photonics, Inc. This APD array comprised 16 line elements, each with 0.3x8 mm^2 area on a 0.5mm pitch. The array was operated at bias voltage of around 1700V, with all channels connected via ac coupling to the front-end ASIC. The array has a dark current of 4 nA and capacitance of 6pf per channel. Figure 10 shows a weighted mean position calculation using all digitized signals using data obtained from direct x-ray interactions in the APD pixels. Using all channels for positioning events is unnecessary for x-ray direct interactions but was done in this case to access both the degree of inter-pixel noise and sensitivity variation in one plot. The good response uniformity is evident from this plot. The sharp peaks at the pixel locations indicate a low level of un-correlated pixel noise, which will be important for positioning events with a scintillation crystal sheet, where light is shared over elements.

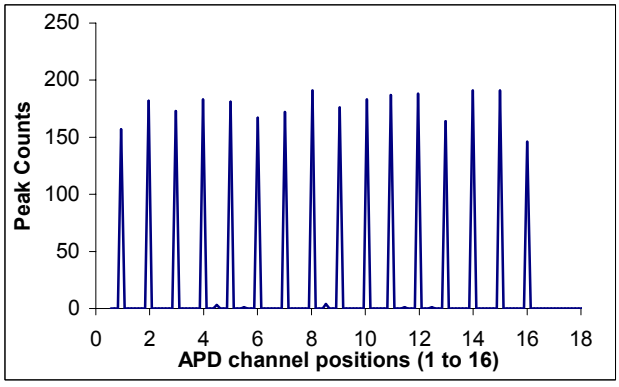

Figure 10: Weighted mean x-ray response over 16 channels.

A single channel measurement with direct x-ray interactions (Figure 11) provided an energy resolution of 13% of FWHM at 5.9 keV, which is comparable to that obtained with a standard discrete charge sensitive preamp/shaper circuit [7]. Preliminary performance measurements using a LSO scintillation crystal sheet have been performed in another report [7].

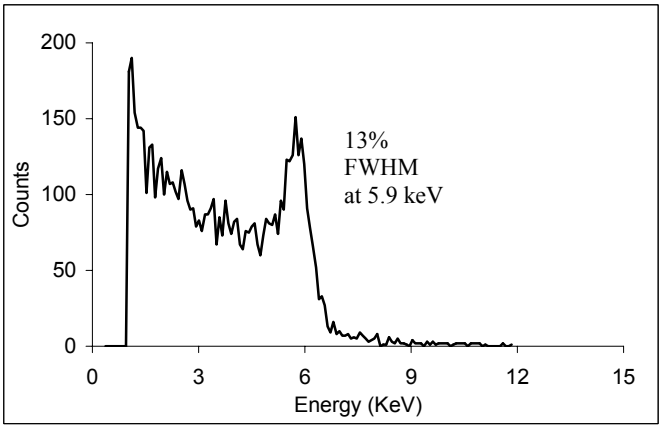

Figure 11: X-ray spectra for 1 ASIC channel

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VII. Discussion and Conclusion

Preliminary performance measurements indicate that the front-end ASIC tested has excellent performance with stable noise and gain uniformity. Initial results with APD arrays connected to the ASIC also showed good signal uniformity and relatively low noise. The fact that the ASIC works well with the two different prototype APD arrays shows that these commercially available ASIC circuits are versatile and may be used in the proposed design. More detailed evaluation of the ASIC, and its capabilities to readout APD arrays, in particular with regard to spatial, energy, and temporal resolutions using a scintillation crystal sheet are being performed. The design of a complete readout system based on such front-end ASICs and additional separate acquisition and processing units are also under investigation.

VIII. Acknowledgment

The authors would like to thank R. Farrell at RMD, Inc. and M. Szawlowski at Advanced Photonics for useful discussions and providing APD array samples, and Dr. B. Sundal for useful discussions and support with regarding to the front-end ASIC .

IX. References

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