Study of Low Noise Multichannel Readout Electronics for High Sensitivity PET Systems Based on Avalanche Photodiode Arrays

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***Abstract*—A compact, low noise, and low cost readout system based on commercially available application-specific integrated circuits (ASICs) is under investigation. These front-end circuits have been used to readout a prototype detector module comprising Lutetium Oxyorthosilicate (LSO) scintillation crystals coupled to avalanche photodiode (APD) arrays. A major goal for this work is to build a dedicated high performance breast imaging PET system. Characteristics of signal response, noise, pedestals and gain of the chip have been evaluated. The channels have a linear response to within 2% across a ± 50 fC dynamic range. The circuits allow hardware adjustment of bias levels to allow gain uniformity of less than 5% for all channels within a chip and the gain performance is very stable over all channels. Initial tests of the chip when connected to a prototype APD array also showed good performance. 13% energy resolution was obtained with direct 5.9 keV X-ray interactions in an individual APD pixel. Initial performance evaluation indicates that the ASIC may serve as a foundation for front-end readout electronics for the proposed PET system.**

***Index Terms*—Application specific integrated circuit, avalanche photodiode, multichannel readout, PET system.**

I. Introduction

THERE is a considerable demand in recent biomedical research to improve the spatial resolution of positron emission tomography (PET) systems [1]–[5]. The spatial resolution of PET imaging depends on several limiting factors such as detector size, annihilation photon noncollinearity, and positron range [6]. Recent work [7] suggests that high spatial resolution can be achieved using compact and highly pixellated avalanche photodiode (APD) arrays coupled to fine LSO scintillation crystals. APDs are currently popular in many applications [8]–[11] and are particularly appealing for high resolution PET system design due to their compactness, high quantum efficiency, good spatial uniformity, insensitivity to magnetic fields, flexible geometric configuration, and potentially low cost.

A novel detector configuration has been proposed which exploits the high compactness of APDs [12]. In this design concept, APD readout arrays are coupled to the side face of fine LSO crystals rather than to the end faces. This new coupling scheme provides nearly complete $(\sim 95\%)$ scintillation light collection efficiency in order to preserve high detector signal-to-noise ratio (S/N). Based on this design, ultra-high resolution, high sensitivity PET systems are being developed for breast and small animal imaging.

This paper describes the study of readout electronics for the proposed PET system based on compact APD detector modules. One design for the prototype APD arrays requires individual channel readout to provide best spatial and energy resolution. In order to practically manage a relatively large number of such readout channels, low noise and low power integrated front-end readout electronics optimized to a particular design configuration are required. Recently, low noise and low power application specific integrated circuits (ASICs) have been designed for certain types of APD arrays [13], [14]. However, these designs are not currently commercially accessible for our application. On the other hand, there are ASIC chips available commercially [15], [16] that have been designed initially for other applications but which have many interesting features that can be used with the state-of-the-art APDs. This work focuses in evaluating such chips for the development of a compact, low noise and low cost front-end readout.

II. Proposed PET System and Readout Requirements

Fig. 1 depicts the proposed design of small, high sensitivity PET systems, which are being developed for breast and small animal imaging. The PET systems will be built using several 1-D detector modules, each consisting of a very thin $(\leq 300\ \mu\mathrm{m})$ APD array coupled to a very thin rectangular LSO crystal sheet. These detector layers are stacked together and placed "edge on" with respect to incoming photons.

The prototype detector module uses an APD array that comprises 41 rectangular elements, each with dimension of $0.7 \times 7\ \mathrm{mm}^2$ on a 1 mm pitch. The final APD array module will be $\leq 300\ \mu\mathrm{m}$ thick and more compact with more channels. In this prototype design, individual APD channel readout is selected in order to provide optimal spatial and energy resolutions. To efficiently manage a large number of channels involved in the design and significantly reduce heat generation in the system, integration of many of the APD channels into a low power and low noise ASIC front-end chip optimized for the system is necessary. In this work, the possibility of utilizing commercially available multichannel front-end chips is investigated in order to significantly reduce the development time and cost.

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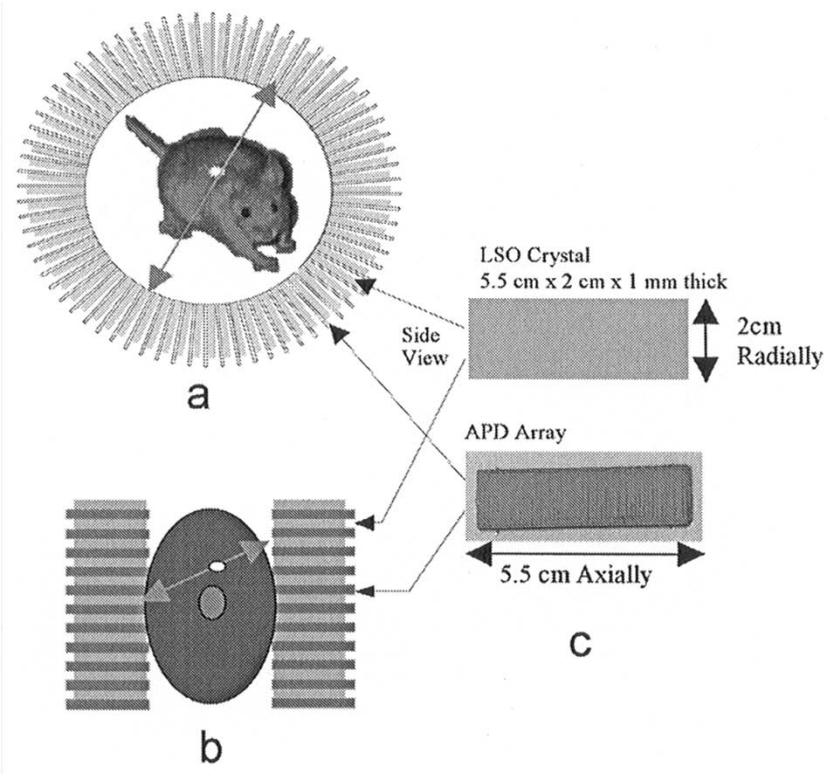

Fig. 1. Depiction of small PET designs for: (a) small animal and (b) breast imaging systems and (c) prototype 1-D array detector module comprises an LSO crystal sheet coupled to an APD array.

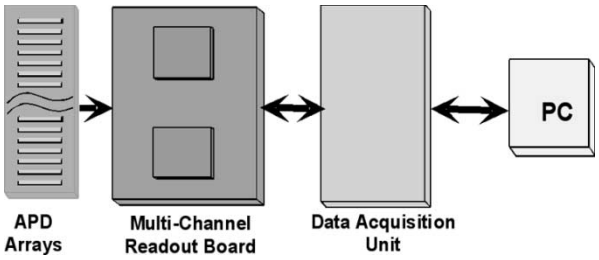

Fig. 2. Prototype readout system setup.

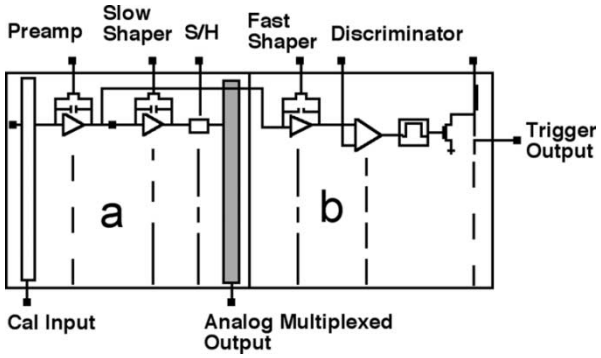

Fig. 3. Front-end ASIC architecture.

III. Prototype Readout System Setup

A prototype multichannel readout system has been setup as indicated in Fig. 2. A prototype APD detector array is connected to a multichannel readout board (IDEAS ASA), hosting two ASIC chips. Each ASIC chip consists of 32 input readout channels that can operate independently. The output from each channel is multiplexed and readout serially by a data acquisition unit, which is interfaced to a PC for processing.

All channels can also be tested through a multiplexed input that allows injecting a test charge into a specific channel. External bias adjustment is provided for calibration purposes. The board allows control and measurement of fundamental parameters of the chip, which includes pedestal, noise, and gain. The internal architecture of the chip is illustrated in Fig. 3.

IV. The Front-End ASIC Chip

The front-end readout ASIC chip is based on the VA/TA chip series from IDEAS, Norway. A single VA/TA chip includes 32 channels of a parallel analog readout circuit followed by a corresponding analog trigger circuit. A summary of typical specifications for the selected chip is shown in Table I.

A single channel includes a low power charge-sensitive preamplifier, slow shaper, sample/hold, and fast trigger circuits (Fig. 3). The trigger chip includes a fast CR-RC shaper followed by externally adjustable level-sensitive discriminator. A signal above the threshold level generates a trigger signal, which is ORed to provide a single trigger output.

The timing and signal acquisition sequence is depicted in Fig. 4. The output signal from the preamplifier circuit is fed simultaneously to slow and fast shaper circuits. The fast shaper output passes through the discriminator and generates a trigger signal if the input signal is above pre-set threshold value. This trigger signal is fed back to analog circuit and enables the sample/hold signal to sample the data simultaneously. The data

TABLE I
VA/TA SUMMARY OF SPECIFICATIONS

Supply Voltage	± 2V
Feedback resistor	Adjustable (~ 10MΩ -10GΩ)
Input Device	PMOS referenced to ground
Peaking time	1.5μS - 3μS (typical ~2μS)
Capacitive load	< 10 pF
Noise	$100e^{-}$ + $15e^{-}$/pF
Typical gain	~8.3 μA/ fC
Gain Range	< 10% of Mean
Pedestal Range	< 4.5% of full range
Max. Readout speed	10 MHz

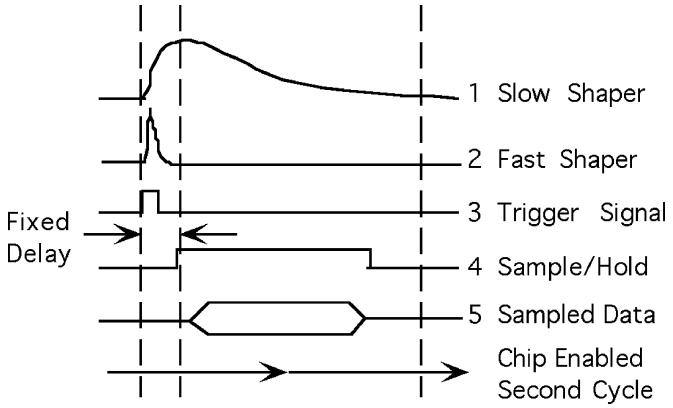

Fig. 4. Signal acquisition sequence.

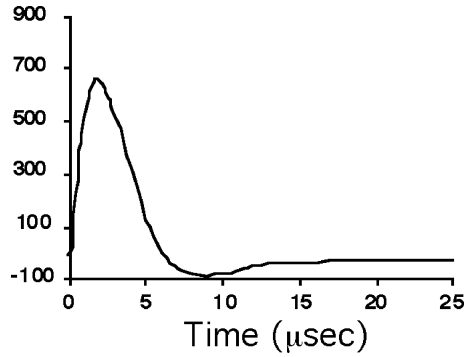

Fig. 5. Preamp/Shaper signal response for one channel.

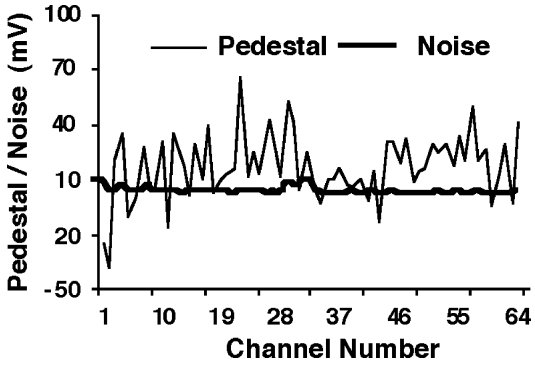

Fig. 6. Pedestal and noise variation between ASIC channels without APD array connected.

is then acquired sequentially through the multiplexed output to the acquisition unit, which is interfaced to a PC for processing. Once the data is read, the sample/hold circuit is disabled to allow acceptance of the next event.

V. ASIC PERFORMANCE TEST MEASUREMENTS

Evaluation measurements have been performed to test the intrinsic performance of the ASIC using a digital test pulse. A digital voltage step was applied via external 1.8 pF capacitor to a calibration input of the chip. This provided a test charge input that was accessible to all channels via the input multiplexer that operates in parallel with the output multiplexer. This process is controlled via 32-bit shift register included in the chip. The test signal was also applied to one selected channel at a time to observe individual channel response of the chip.

Fig. 5 shows a semi-Gaussian shaped signal response from a typical channel in the preamp/shaping circuit. The typical peaking time for this particular chip is 2 μs, with the possibility of external bias adjustment to extend the range from 1.5 to 3 μs. This value is clearly not optimal for a detector based upon LSO crystal, which has a scintillation decay time of 40 ns. The relatively large peaking time will introduce unnecessary dead time, limiting the count rate performance, and may add unnecessary noise into the system due to its relatively long integration period. The new generation chips of this series and similar compatible families are expected to have more appropriate peaking time for LSO with good noise performance.

Fig. 6 shows the noise and pedestal measurements for all channels. The values are obtained by a multiplexed readout sequence, where a hold is applied and a consecutive sampling of the shaped signals has been performed and averaged. The intrinsic noise of the chip is uniform over all channels to within $\pm 10\%$. The pedestal represents the minimum detected pulse height for a given channel. Pedestal spread is relatively large ($>15\%$ of the average pulse height) but may be corrected in software.

External bias adjustment keeps the gain variation between channels in a single chip to less than 5% (Fig. 7). There is a $\sim 10\%$ variation in gain between the two 32-channel circuits that may be corrected in post-processing.

The linearity as function of input test charge that mimics a 511 keV photon LSO-APD signal for one channel of the ASIC was measured using an external pulser. In this case the test mode operation was disabled to enable the input channels to accept external signals. The charge amplitude was obtained from the peak location in the pulse height spectrum. The response was linear to within 2% for a ± 50 fC dynamic range (Fig. 8).

Again new generation of this chip is expected to have better linearity and better dynamic range. For a 511 keV photon interacting in LSO, coupled to an APD array (gain $=$ 1000), the estimated dynamic range required is ± 1.3 pC in order to fully utilize the charge signals from each event. This is however above the dynamic range of the ASIC chip being evaluated ($\sim \pm 80$ fC). We thus, had to implement a terminating resistor (10–20 MΩ) to drain enough of the signal charge to be within the linear region of the input dynamic range of the chip.

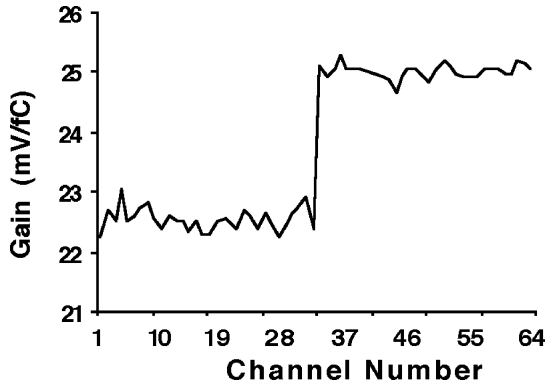

Fig. 7. Gain variation between channels.

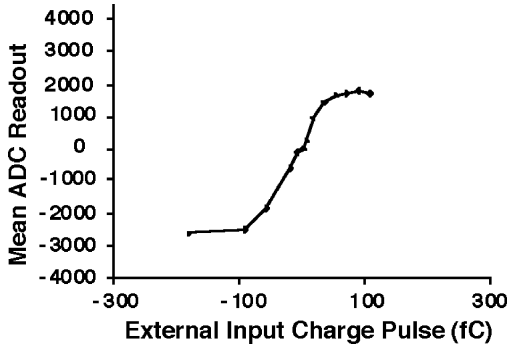

Fig. 8. Linearity and dynamic range performance test.

VI. Initial Tests and Results With APD Arrays Connected

So far we have discussed intrinsic performance of the readout ASIC without connecting the APD array. These intrinsic measurements do not include the leakage current, detector capacitance and overall APD detector dark noise that significantly affect the overall performance of the system. To study the basic performance of the chip connected to APD arrays, two newly developed prototype 1-D APD arrays were used. The APDs had different configurations and characteristics. All measurements were performed using a 5.9 keV Fe-55 X-ray source. These measurements were used to study the overall capabilities and limitations of this particular existing ASIC for reading out the particular APD arrays we have in mind. We expect that in the final system, we will need to customize a similar chip to optimize performance for our particular application.

The first measurement was performed using a prototype APD array obtained from RMD, Inc [17]. This array consists of 41 APD elements, each with $0.7 \times 7\ \mathrm{mm}^2$ on a 1 mm pitch. At bias voltage around $V_{\mathrm{bias}} = 1100$ V, it has a stable gain with dark current of about 50 nA and capacitance of $0.7\ \mathrm{pf/mm}^2$. In this particular APD array eight elements (channels) were used that had easily accessible pins to connect to the prototype ASIC board. Each channel was connected to the front-end ASIC using ac-coupling due to the relatively high leakage current of the APD. The detector input was also terminated with a 10–20 $\mathrm{M}\Omega$ resistor to drain the leakage current and attenuate the signal so that the resulting signal falls within the linear dynamic range of the ASIC. A second prototype APD array was obtained from Advanced Photonix, Inc. (API) [18]. This APD array comprised 16 line elements, each with $0.3 \times 8\ \mathrm{mm}^2$ area on a 0.5 mm pitch. The array was operated at bias voltage of around 1700 V, with all terminated channels connected via ac-coupling to the front-end ASIC. This array has relatively lower dark current (4 nA) and capacitance of 6 pf per channel. A terminating resistor of 10 $\mathrm{M}\Omega$ was used for this APD array to drain the leakage current.

A. Energy Measurements

Fig. 9 shows the energy spectrum obtained for both APDs with direct X-ray interactions. Energy resolution of 14.6% and 13% of FWHM at 5.9 keV was achieved respectively using RMD Inc and Advanced Photonix APD. Due to higher leakage current per channel the energy resolution obtained using the RMD Inc APD is slightly worse than that of Advanced Photonix. However, both results are comparable to that obtained with a standard discrete charge sensitive preamp/shaper circuit [7].

B. Gain Uniformity

The response of eight channels superimposed for the RMD array is shown in Fig. 10. The plot shows that uniformity between channels is maintained to within 5% gain variation, even when the APD array is connected to the ASIC.

C. Positioning Measurements

Fig. 11 shows a Fe-55 X-ray flood field position histogram using the 16 channels Advanced Photonix APD array, which has all 16 channels easily accessible to connect to the prototype readout board. Each direct X-ray interaction in the silicon APD pixels was positioned with a weighted mean position calculation involving all digitized signals from each event. Using a weighted mean over all channels for positioning X-ray direct interactions is unnecessary but was done in this case to access both the degree of APD array pixel noise and sensitivity variation in one plot.

Good response uniformity is evident from this plot. The sharp peaks at the pixel locations in this weighted mean positioning histogram indicate that the level of uncorrelated pixel noise is very low. This low pixel noise will be important for positioning events with a scintillation crystal sheet since multiple elements are involved in positioning an event. Preliminary performance measurements using a LSO scintillation crystal sheet coupled to the RMD array have been reported in another paper [7].

VII. Future Readout System Design and Strategy

The future readout electronics design will be a tradeoff between an optimized ASIC solution with respect to performance parameters such as noise, gain, power consumption, linearity and uniformity and its development cost. For a full readout system the primary design goal is to utilize as much as possible commercially available front-end electronics. A programmable dedicated readout system (Fig. 12) will be developed based on FPGA and DSP components in order to have a flexible

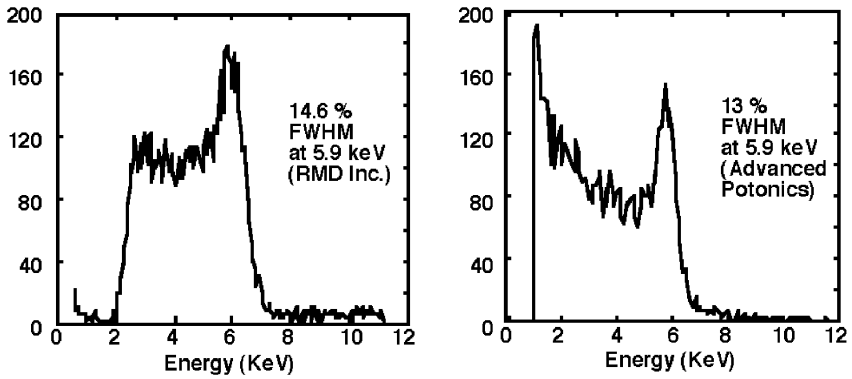

Fig. 9. X-ray spectra for single ASIC channel. Left, using RMD, Inc. APD and Right, using advanced photonix APD.

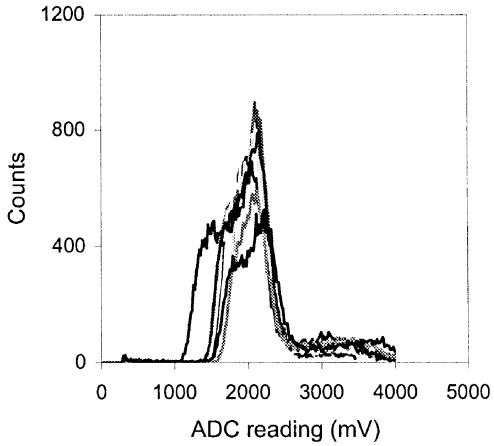

Fig. 10. Measured X-ray spectra in eight APD channels.

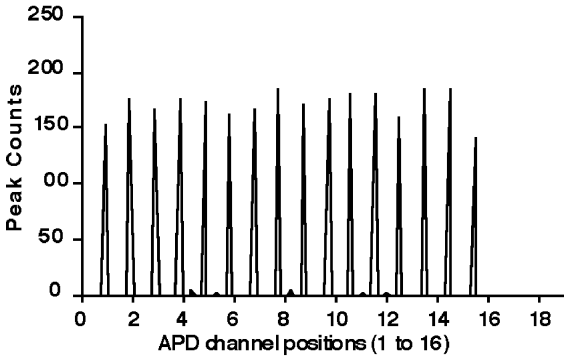

Fig. 11. Weighted mean X-ray position response over 16 channels from advanced photonix APD array.

hardware system that can support future development of the front-end electronics.

The design strategy will be based on a modular design to simplify the design complexity and easily upgrade the system based on the modifications are required. The front-end readout module will host several APD array readout ASICs, each connected to a fast digitizers. The digitized data will be forwarded to an FPGA/DSP unit for efficient digital processing and storage of detector signals. The trigger system, energy discrimination and coincidence identification will be implemented in the FPGA. A control and PC interface board will manage all modules and implement the data transfer protocol from and to the PC.

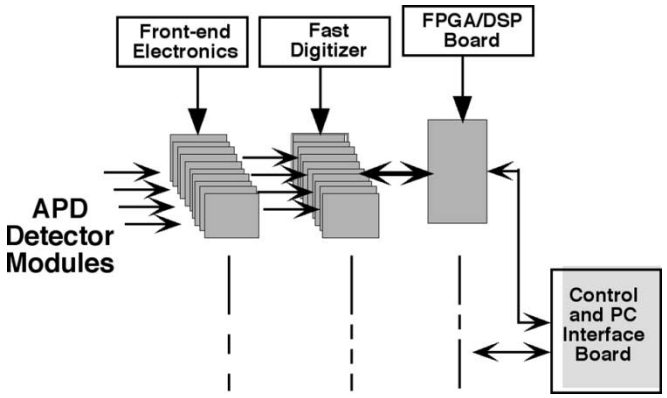

Fig. 12. Depiction of future readout system design.

VIII. Discussion and Conclusion

Preliminary performance measurements indicate that the front-end ASIC tested has excellent performance with stable noise and gain uniformity. Initial results with APD arrays connected to the ASIC also showed good signal uniformity and relatively low noise. The fact that the ASIC works well with the two different prototype APD arrays shows that these commercially available ASIC circuits are versatile and may be useful in the proposed design. More detailed evaluation of the ASIC, and its capabilities to readout APD arrays, in particular with regard to spatial, energy, and temporal resolutions using a scintillation crystal are being performed. The design of a complete readout system based on such front-end ASICs and additional separate acquisition and processing units are under investigation.

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